In the Claims:

1-16. (canceled)

17. (previously added) An integrated circuit comprising:

A. functional circuitry having data input leads and data output leads;

B. test access port circuitry having a test data input lead, a test data output lead, a test mode select lead, a test clock lead, scan circuitry control output leads, and a data register connected in series between the test data input lead and the test data output lead, the data register having a serial data output lead and a serial data input lead;

C. scan test port circuitry having a scan input lead connected to the serial data output lead, a scan output lead connected to the serial data input lead, a scan enable input lead, a capture select input lead, a scan clock input lead, and a scan register connected between the scan input lead and the scan output lead, the scan register having functional data output and input leads connected to the functional circuitry data input and output leads;

D. connection circuitry coupling the scan test port circuitry to the test access port circuitry, the connection circuitry having inputs connected to the scan circuitry control output leads, the test mode input lead, the test clock input lead, and the connection circuitry being connected to the scan enable input lead, the capture select input lead, and the scan clock input lead;

E. a first gate selectively connecting a test mode signal to the test mode lead, the first gate including a lock out

signal input, the lock out signal selectively controlling coupling the test mode signal to the test mode lead; and

F. tap lock circuitry having a lock out signal output connected to the lock out signal input of the first gate, the tap lock circuitry having inputs connected to the test access port circuitry, the test mode select signal, and the test clock lead.

18. (previously added) The integrated circuit of claim 17 in which the tap lock circuitry has an input connected to an UPDATE-IR signal from the test access port circuitry.

19. (previously added) The integrated circuit of claim 17 in which the tap lock circuitry includes a flip-flop, an AND gate, an unlock state machine and an inverter, the flip-flop receives a lock-in signal from the test access port at a data input, an UPDATE-IR signal from the test access port at a clock input, and the output of the AND gate at a reset input, the normal data output of the flip-flop is input to the inverter, the output of the inverter is the lock out signal, the unlock state machine receives the test mode select signal at a data input, the normal data output of the flip-flop at an enable input, the test clock signal at a clock input, and a test reset signal at a reset input, the unlock state machine provides an unlock output as an input to the AND gate, and another input to the AND gate is the test reset signal.

20. (previously added) The integrated circuit of claim 17 in which the tap lock circuitry includes a state machine having a data input connected to the test mode select signal.